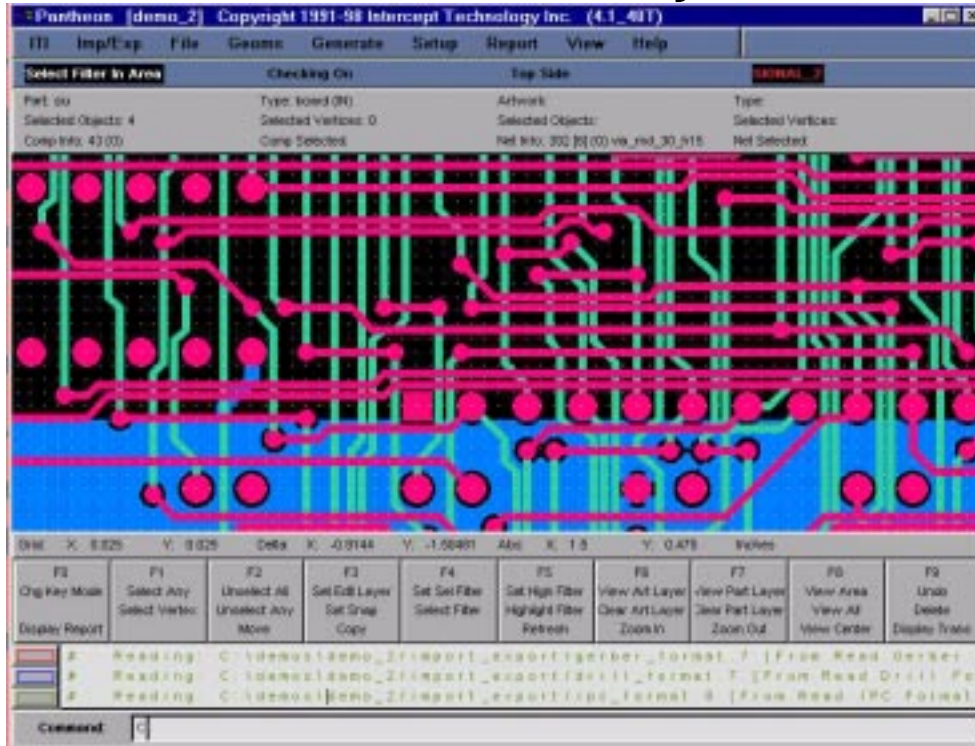


INTERCEPT

Pantheon Product Family



Overview

Pantheon™ gives you the most advanced features in PCB layout available in the industry today whether you're desinging simple boards or extremely dense, mixed-pitch, multi-layer designs with high-component counts and mixed signal technology. Features include shape-based interactive routing, WYSIWYG capabilities, complex area fills, split power planes, embedded traces, and complete manufacturing output, all with the interactive control that gives you the results you want, *fast*.

Pantheon family products include comprehensive reporting and plotting capabilities. Plus, they all work seamlessly with SPECCTRA® Autorouter, OrCAD Express™, OrCAD Capture™, and Design Architect™ products to automate information-sharing and reduce the number of back-and-forth passes between engineer and board designer. Intercept Technology's Pantheon family offers tightly integrated, complete solutions for designing boards of all complexities.

With Pantheon, net and component data update automatically as modifications are made. Additionally, comprehensive design and manufacturing database verification are included to insure design integrity. Capabilities such as cutouts and outlines in area fills are supported for Gerber(X), IPC-D-350C, IPC-D-356, DXF, and Artwork 2000 (a public domain manufacturing database developed by Intercept).

Pantheon Product Family Features

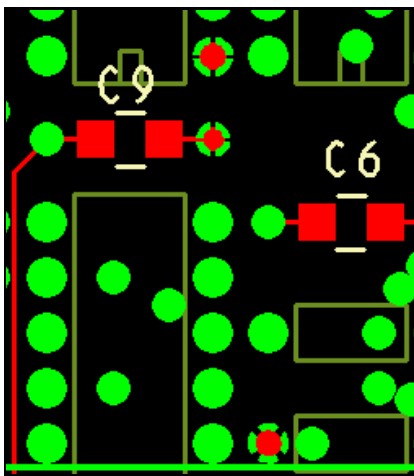
Features	Pantheon	Designer	Geometer	CPR	Viewer
Database Viewing	◆	◆	◆	◆	◆
DRCs	◆	◆	◆	◆	
Manufacturing Verification	◆				
Area Fills	◆	◆			
SPECCTRA Interface	◆	◆			
Artwork Generation	◆	◆			
Import Artwork	*	*			
Plotting & Printing	◆	◆	◆	◆	◆
RF Interface (IFF)	*	*			
High Speed Design	*	*			
IDF	*	*	*		
Schematic Interfaces	◆	◆	◆	◆	◆
GenCAD	◆	*			
DXF Database	*	*	*		
PERL Extensions	◆	◆	◆	◆	◆

Key: ◆ Included Feature * Optional Software

Pantheon Features

High Technology Design

Pantheon includes complete design layout and artwork generation capabilities. Within a single design environment, Pantheon offers geometry creation, interactive component placement and routing, complex area fill generation, testpoints, tear drops, PCB design checks, artwork generation, and manufacturing verification.



Complete WYSIWYG Features

With powerful and intuitive WYSIWYG design technology, Pantheon includes buried vias, blind pins, split power planes, embedded and curved traces, circular area fill cutouts and outlines, and automatic and interactive generation of tear drops and testpoints.

Flexible Geometry Creation

Designers can easily create every type of geometry, including drawings, panels, boards, pins, vias, and components. If existing geometries require modification, Pantheon also includes powerful editing commands. Designers can copy or rename geometries, or delete actively used parts or parts

unreferenced in the Pantheon design.

Designers can also make use of Pantheon's geometry library features. Users can load geometries from existing libraries, or they can compare geometries in the Pantheon database to those in a library to check for modifications or discrepancies.

Intuitive Component Placement

In Pantheon, designers define every aspect of component placement. Users can specify component to component placement clearance through a default template or use flexible component clearance rules and classes.

Users can also define the display of component objects during placement. And with component mapping, Pantheon displays all unplaced components off-board to ease the component placement process.

Pantheon includes complete editing capabilities for placed components. Users can unplace, flip, rotate, align, move, swap, or change component part names or symbols as needed. And designers can reorder component references on both board sides sequentially or simultaneously.

Interactive Routing

In Pantheon, designers use comprehensive rules to define routing clearance for pins, vias, and traces. Minimum allowed wire width, wire direction, and minimum fill width are also defined.

During interactive routing, widths and clearances are rules-driven. Additionally, a single guide auto-router is included to speed initial routing of the board. Automatic routing is also available through an interface with the SPECCTRA® shape-based autorouter. Integration of the Zuken-Redac Route Editor is planned.

WYSIWYG Area Fills

Pantheon also includes powerful area fill capabilities for automatic and interactive WYSIWYG area fill generation. Pantheon supports and displays circular cutouts, hatching, and cross-hatching. Pantheon can also include thermals in area fill generation.



Thermals and Smooth Area Fill Cutouts

Once area fills are created, designers can modify any aspect of existing area fills, from cutout segments to thermal properties. And when routing is modified, Pantheon allows plowing and healing of area fills.

Schematic & Layout Driven Designs

If a change is required in a design during layout, designers can modify the board without returning to the schematic. Users can fully edit or add net connectivity and add or delete components.

When modifications are made, Pantheon uses advanced comparison tools to resolve discrepancies. With Pantheon, the forward or reverse design methodology is left to the designer, giving users the power to create without returning to the schematic.

Double Verification

Ensure Design Integrity

Double verification increases the likelihood of success by checking both the PCB design and manufacturing databases. With Pantheon's comprehensive and rigorous PCB design and manufacturing rule checks, designers never have to worry about manufacturing a bad board.

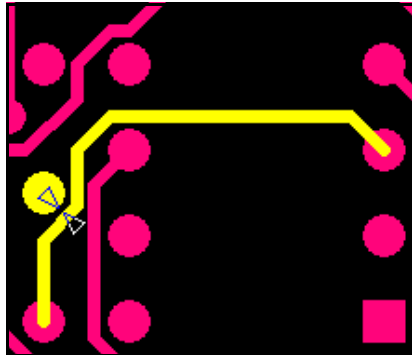
Designers can easily create and define their own PCB design rule definitions, including a flexible set of net, component, and padstack rules and classes. As designers layout a design, Pantheon automatically checks the printed circuit board against the predefined design rules.

Pantheon's manufacturing verification contains a complete matrix of object clearance checks, including verification of annular rings, anti-pads, and soldermask coverage. Pantheon creates a report of all violations and displays errors individually or all at once.

Design on Time with ZDD

Double verification ensures Zero Design Defects (ZDD) on the first pass. Pantheon's on-screen, WYSIWYG verification feature

allows designers to check the design's PCB and manufacturing data for any errors before the design goes into fabrication.



Manufacturing Violation

Pantheon features save days or weeks of wasted time, shortening the development cycle and reducing the risk of costly delays. The double verification process reduces the number of redesigns and improves design quality.

PCB Design Verification

Pantheon includes a complete set of database design rule checks. Designers can fully verify routing, net topology, area fills, tear drops, testpoints, geometries, component placement, and physical layers.

Pantheon can check geometries for all required and invalid

attributes, references, and dimensions. Components are checked for valid or duplicate references, and for geometry or placement violations. Designers can also check nets for clearance and constraint violations, including padstacks and traces within routing outlines, minimum wire width, and allowed wire direction. Pantheon also checks for floating area fills or antenna traces.

All violations are compiled in a tabulated report with a brief summary of each violation. Designers can display the report or output it to a file. Pantheon can display each violation separately on-screen to assist in problem resolution.

Manufacturing Verification

In Pantheon, designers perform checks on the actual manufacturing database files. The manufacturing rule checks (MRCs) report and flag clearance, constraint, and coverage violations.

With Pantheon's MRC Lite dialog boxes, the setup of manufacturing rules is fast and easy. MRCs are divided by clearance, coverage, drill and power/trace. Each category has its own dialog box to create and modify each MRC category.

Pantheon also offers an expanded set of dialog boxes for designs that require more complex or advanced MRCs.

Electrical Rule Checks

In Pantheon, electrical rule checks (ERCs) provide effective electrical verification of manufacturing data. Through a process called assigning artwork, Pantheon creates an artwork node list, the equivalent of a PCB net list. The node list is compared against the PCB net list. Results indicate mismatched nets, shorts, opens, extra pins, and missing pins in the manufacturing data.

Manufacturing Rule Check (MRC) Examples

MRC Class	MRC Functions				
Object Clearances Matrix	Pin-Pin	Pin-Via	Pin-Wire	Pin-Fill	Pin-Misc
		Via-Via	Via-Wire	Via-Fill	Via-Misc
			Wire-Wire	Wire-Fill	Wire-Misc
				Fill-Fill	Fill-Misc
					Misc-Misc
Plane Constraints	Minimum Width		Islands		
Power Isolation	Thermal Spokes		Minimum Connections		
Trace Constraints	Wire Direction		Minimum Wire & Fill Width		

Pantheon Interfaces

Complete Design Solution

Pantheon offers the seamless transfer of design information to and from several schematic entry and manufacturing applications. For most schematic entry interfaces, Pantheon requires only nets and component files to transfer all schematic design information and to start the layout process.

Pantheon also interfaces to HP EEsof™ applications for RF design and to the GenCAD manufacturing file format.

OrCAD Interface

Pantheon can read and write component, gate, and net information to OrCAD Capture™ or Express™ for schematics done in OrCAD's schematic entry programs. From OrCAD, a comps file containing a list of design components and related information (such as placement attributes) can be written and brought into Pantheon.

Pantheon also includes inter-application communication with cross-probing. This feature allows design information to be shared simultaneously in Pantheon and OrCAD. As designers select a component in Pantheon, the

component is automatically selected in OrCAD. Additionally, as a part is selected in OrCAD's schematic, Pantheon also selects the geometry.

Mentor DA

Designers can use a schematic from Design Architect™ to drive a PCB's netlist connectivity and component placement information in Pantheon. Symbols in a DA schematic can become parametric RF elements in Pantheon, which can then be written out in an HP EEsof IFF design file. Designers can modify placement or properties of RF components. Users can also backannotate the completed design properties to update the schematic in DA.

Viewlogic Interface

Pantheon can read and write component, gate, and net information directly from the Viewlogic™ schematic entry program.

In the forward annotate process (PCBFWD), Pantheon-compatible design files are written from Viewlogic and read into Pantheon. Designers can transfer a list of

design components and related attributes, and physical to logical mapping information for each gate instance in the design. Designers can also transfer information on swappable gates and pins and on component pin connections.

In the backannotate process (PCBBCK), designers translate the design information for use in Viewlogic.

GenCAD Interface

Pantheon offers an interface to the GenCAD file format used in Mitron's CIMBridge Manufacturing Framework.

Designers can transfer information seamlessly from the Pantheon design database to the GenCAD manufacturing engineering group. Support of the GenCAD file format in Pantheon eases the creation and assembly of products with short life cycles and time to market constraints.

Interface Features

Interface	Cross-Probing	Back-Annotation	Design Variants
Design Architect	*	◆	◆
OrCAD Capture	◆	◆	*
ViewLogic		◆	◆

Key: ◆ Available. * Planned.

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SPECTRA is a registered trademark of Cadence.
Viewlogic is a registered trademark of Viewlogic Systems Inc.
HP EEsof is a registered trademark of Hewlett-Packard Company.

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